

REMARKS

In the outstanding Office Action, the Examiner rejected claims 1-8 under 35 U.S.C. §102(b) as being anticipated by Kazerounian et al., U.S. Patent No. 5,006,974 (hereinafter, Kazerounian). Applicant respectfully traverses this rejection for at least the reasons given below.

Independent claim 1 recites in part “wherein the multiplier comprises a switching capacitor circuit (21) coupled between input (31) and output (32) terminals of the multiplier, said switching capacitor circuit (21) provided with capacitors and *switches for charging the capacitors in parallel and discharging them in series in order to deliver a high voltage pulse*” (emphasis added). Applicant can find no disclosure in Kazerounian of the recited subject matter from independent claim 1.

In the outstanding Office Action, the Examiner appears to assert that the charge pump circuitry 128 of Kazerounian is equivalent to the claimed “switching capacitor circuit”. Applicant respectfully disagrees. In Kazerounian, the element 128 (called a “switching network”) and the capacitors 120, 122, and 124 solely produce a stable reference voltage, V_{ref} on lead 118. See the discussion from col. 8, line 52 to col. 9, line 38 of Kazerounian. In particular, see col. 8, lines 65-68 of Kazerounian, where it states: “The network including capacitors 120-1 to 120-20, 122-1 to 122-10, 124-1 to 124-10 and switching network 128 controls voltage V_{REF} to a desired value.” Additionally, the nonvolatile register 106 controls V_{REF} (col. 8, lines 63-65 of Kazerounian) and V_{REF} is selected (using register 106) to be a particular value using a certain process. See Kazerounian at col. 8, line 68 to col. 9, line 48 of Kazerounian. These elements (128, 120, 122, and 124) in Kazerounian therefore do not deliver a high voltage *pulse*, as claimed in independent claim 1 herein.

Further, the capacitors 124 are not charged in parallel and discharged in series, as recited in independent claim 1. Instead, capacitors 124 are selected initially as being coupled to ground through switches 126 and then one at a time they are coupled to V_{pp} until

an appropriate erasing voltage is produced at output 104. The output voltage 104 is adjusted because the comparator 116 produces a binary output signal (a “one”) on output lead 119, which causes ring oscillator circuit 124 (incorrectly marked in the drawings as “123”) to ring and produce the signals ϕ and $\bar{\phi}$. When $V_{out}/4$ is less than V_{ref} , the comparator produces a “zero” on output lead 119, thereby stopping the ring oscillator circuit 124. See Kazerounian at col. 8, lines 9-38.

It should also be noted that element 103 of FIG. 2 of Kazerounian is a voltage multiplier also shown in FIG. 1 of Kazerounian. (Note that the capacitors in voltage multiplier 103 are also marked with a “103”.) Although there are a number of capacitors 103 in the voltage multiplier 103 in Kazerounian, the capacitors 103 do not appear to be charged in parallel and discharged in series and instead are operated using ϕ and $\bar{\phi}$.


Consequently, Kazerounian does not disclose at least the recited subject matter in independent claim 1 of “wherein the multiplier comprises a switching capacitor circuit (21) coupled between input (31) and output (32) terminals of the multiplier, said switching capacitor circuit (21) provided with capacitors and *switches for charging the capacitors in parallel and discharging them in series in order to deliver a high voltage pulse*” (emphasis added). Therefore, Applicant respectfully submits that independent claim 1 is patentable over Kazerounian. Because independent claim 1 is patentable, dependent claims 2-8 are also patentable for at least the reasons given above with respect to independent claim 1.

Based on the foregoing arguments, it should be apparent that claims 1-8 are thus allowable over Kazerounian, and the Examiner is respectfully requested to reconsider and remove the rejections.

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